1. A method for routing a data frame through a fibre channel fabric, said fibre channel fabric comprising a switch having a plurality of ports, said ports are operative for transmitting and receiving said data frame, said method comprising:

receiving said data frame at a first port of said switch;

writing said data frame to a shared memory location, said shared memory location is coupled to at least two of said plurality of ports of said fibre channel switch;

identifying a second port of said switch, said second port operative for transmitting said data frame from said shared memory location;

transmitting a message from said first port to said second port indicating the position in said shared memory location of said data frame; and

at said second port, reading said data frame from said memory, wherein said switch has more than one rate for reading and writing data.

2. The method of claim 1, wherein said shared memory location is implemented using a plurality of SRAM modules, one or more SRAM module for each of said plurality of fibre channel ports.

3. The method of claim 2, wherein said plurality of fibre channel ports is an odd number of fibre channel ports.

4. The method of claim 1, wherein said shared memory comprises a plurality of columns and wherein each of said plurality of fibre channel ports has access to one of said plurality of columns.

5. The method of claim 4, wherein said access occurs during a clock cycle.

6. The method of claim 4, wherein said access occurs during a 106.25 MHz clock cycle.

7. The method of claim 4, wherein said plurality of columns comprises a plurality of SRAM modules.

8. The method of claim 4, wherein said plurality of fibre channel ports have a read access during a first clock cycle and a write access during a second clock cycle, said second clock cycle immediately follows said first clock cycle.

9. The method of claim 1, wherein said shared memory location supports both a 1 gigabit per second and a 2 gigabit per second read and write data rate.

10. A method for providing a shared memory location in a fibre channel fabric, said fibre channel fabric comprising a fibre channel switch having a plurality of fibre channel ports, said fibre channel ports are operative for transmitting and receiving said data frame, said method comprising:

receiving said data frame at a first fibre channel port of said fibre channel switch;

writing said data frame in said shared memory location, said shared memory location coupled to each of said plurality of fibre channel ports; and

reading said frame from said shared memory location into a second fibre channel port, wherein said fibre channel switch has more than one rate for reading and writing data.

and, transmitting said data frame the second fibre channel port, wherein said writing and reading are performed in a manner that is dependent on the relative rates at which said frame is received and transmitted.

11. The method of claim 10, wherein said shared memory location is implemented using a plurality of SRAM modules, one or more SRAM module for each of said plurality of fibre channel ports.

12. The method of claim 11, wherein said plurality of fibre channel ports comprises an odd number of fibre channel ports.

13. The method of claim 10, wherein said shared memory location comprises a plurality of columns and wherein each of said plurality of fibre channel ports has access to one of said plurality of columns.

14. The method of claim 13, wherein said access occurs during a clock cycle.

15. The method of claim 13, wherein said access occurs during a 106.25 MHz clock cycle.

16. The method of claim 13, wherein said plurality of columns comprises a plurality of SRAM modules.

17. The method of claim 13, wherein said plurality of fibre channel ports have a read access during a first clock cycle and a write access during a second clock cycle, said second clock cycle immediately follows said first clock cycle.

18. The method of claim 10, wherein said shared memory location supports both a 1 gigabit per second read and write data rate and a 2 gigabit per second read and write data rate.

19. A fibre channel fabric comprising:

a fibre channel switch having a plurality of fibre channel ports embodied thereon for transmitting and receiving data frames;

a route control module coupled to one of said plurality of fibre channel ports, said route control module for providing an exit port in response to a request from said plurality of fibre channel ports for said exit port, said request comprising a destination identification; and

a memory location, said memory location coupled to each of said plurality of fibre channel ports, wherein said memory location stores data frames transmitted to each of said plurality of fibre channel ports, wherein said fibre channel switch has more than one rate for reading and writing data from said memory location to said each of said plurality of fibre channel ports.

20. The fibre channel fabric of claim 19, further comprising an interface control module that couples a first fibre channel port and a second fibre channel port of said fibre channel switch, wherein said interface control module provides a first control signal to said second fibre channel switch in response to a second control signal from said first fibre channel switch.

21. The fibre channel fabric of claim 19, wherein data frames that are received at a first receiving port of said plurality of ports are written into said memory, and said data frames written into said memory are read from said memory by a first transmitting port of said plurality of ports.

22. The fibre channel fabric of claim 19, wherein said memory comprises a plurality of SRAM modules.

23. The fibre channel fabric of claim 22, wherein said SRAM modules number 17 in total.

24. The fibre channel fabric of claim 19, wherein said memory supports both 1 gigabit per second and 2 gigabit per second read and write data rates.

25. The fibre channel fabric of claim 24, wherein said memory supports a different read rate and write data rate such that data can be written to said memory at a first rate and simultaneously read from said memory at a second, different rate.

26. The fibre channel fabric of claim 19 further comprising a bus coupling said one of said plurality of fibre channel ports to said memory for transmitting said data frame.

27. A method for providing a shared memory location coupled to a plurality of ports in a fibre channel switch for buffering and switching data frames from a first port to a second port, said method comprising:

providing a plurality of columns of memory, said columns of memory comprising a plurality of rows for storing a portion of said data frames, wherein said portion is written from said first port; and

providing a plurality of first-in first out data storage locations, wherein said portion of said data frame is stored in said data storage location before being read to said second port.

28. The method of claim 27, wherein the number of columns of memory is equal to or greater than the number of ports.

29. A method for providing a shared memory location comprising:

receiving data frame at a first port;

writing a first portion of said data frame to a first column of memory;

reading said first portion of said data and thereafter writing said first portion to a first-in first out storage location; and

reading said first portion of said data from said storage location and thereafter writing said first portion to a second port.

30. The method of claim 29, wherein said first portion of said frame comprises a word.

31. The method of claim 30, wherein said word is 34 bits in length.

32. The method of claim 30, wherein said writing to the first column of memory is at a first data rate and the reading from the first column is at a second data rate, wherein said first data rate is different than said second data rate.

33. The method of claim 32, wherein said first data rate is two gigibits per second and said second data rate is one gigibit per second.

34. The method of claim 32, wherein said first data rate is one gigibit per second and said second data rate is two gigibits per second.

35. A shared memory location within a fibre channel fabric having a plurality of ports, said shared memory coupled to said plurality of ports, said shared memory comprising:

a plurality of memory locations, each memory location comprising a column and having a plurality of rows for storing a data frame, said data frame comprising a plurality of words; and

a plurality of first-in first out data storage locations, wherein a word is written from said memory location to said first-in first-out storage location before transmission to a port.

36. The shared memory location of claim 35, wherein the number of memory locations is greater than or equal to the number of ports.

37. The shared memory location of claim 35, wherein the number of memory locations is an odd number.

38. The shared memory location of claim 35, wherein the memory locations are implemented using SRAM modules.

39. The shared memory location of claim 35, wherein the width of said memory location is 34 bits, wherein 34 bits is the length of said word of said data frame.

40. The shared memory location of claim 35, wherein said plurality of said first-in first-out storage locations comprises two first-in first-out storage locations.

41. The shared memory location of claim 35, wherein the depth of a buffer is determined by multiplying the number of frames per port by the number of ports by the number of rows per frame.

42. The shared memory location of claim 35, wherein the number of rows per frame is determined by dividing the frame byte size by the total resulting from multiplying the number of columns by the number of bytes per word.